EEC 289O Lecture #14: Leakage 2

Rajeevan Amirtharajah
University of California, Davis

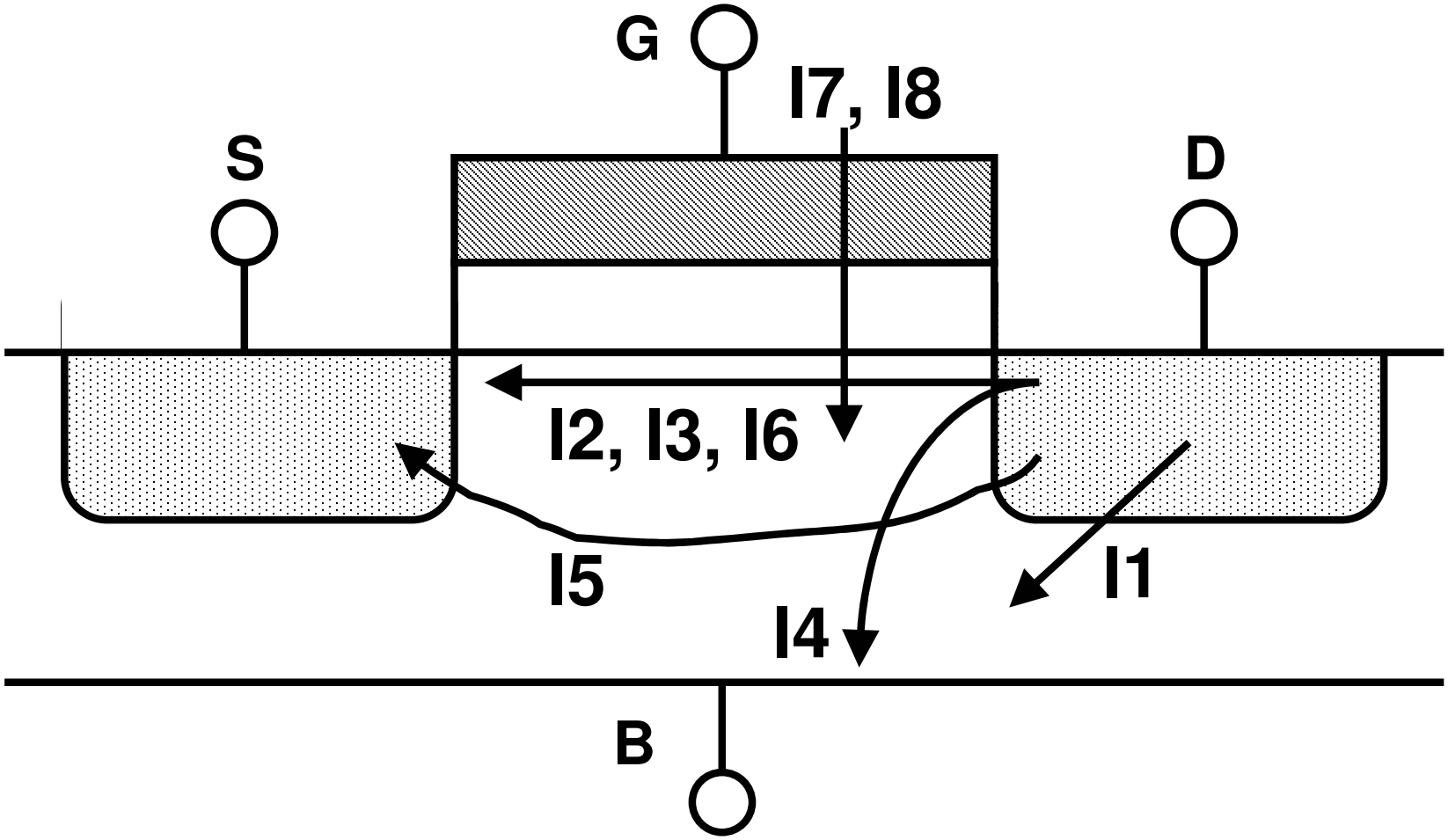
Announcements

- **Midterm Results:**
  - Class Average: 66
  - Std. Deviation: 13.4
  - High Score: 89
- **Rough Curve:**
  - A > 66
  - 66 >= B > 46
  - 46 > C, D, F

Transistor Leakage Mechanisms

1. pn Reverse Bias Current (I1)
2. Subthreshold (Weak Inversion) (I2)
3. Drain Induced Barrier Lowering (I3)
4. Gate Induced Drain Leakage (I4)
5. Punchthrough (I5)
6. Narrow Width Effect (I6)
7. Gate Oxide Tunneling (I7)
8. Hot Carrier Injection (I8)

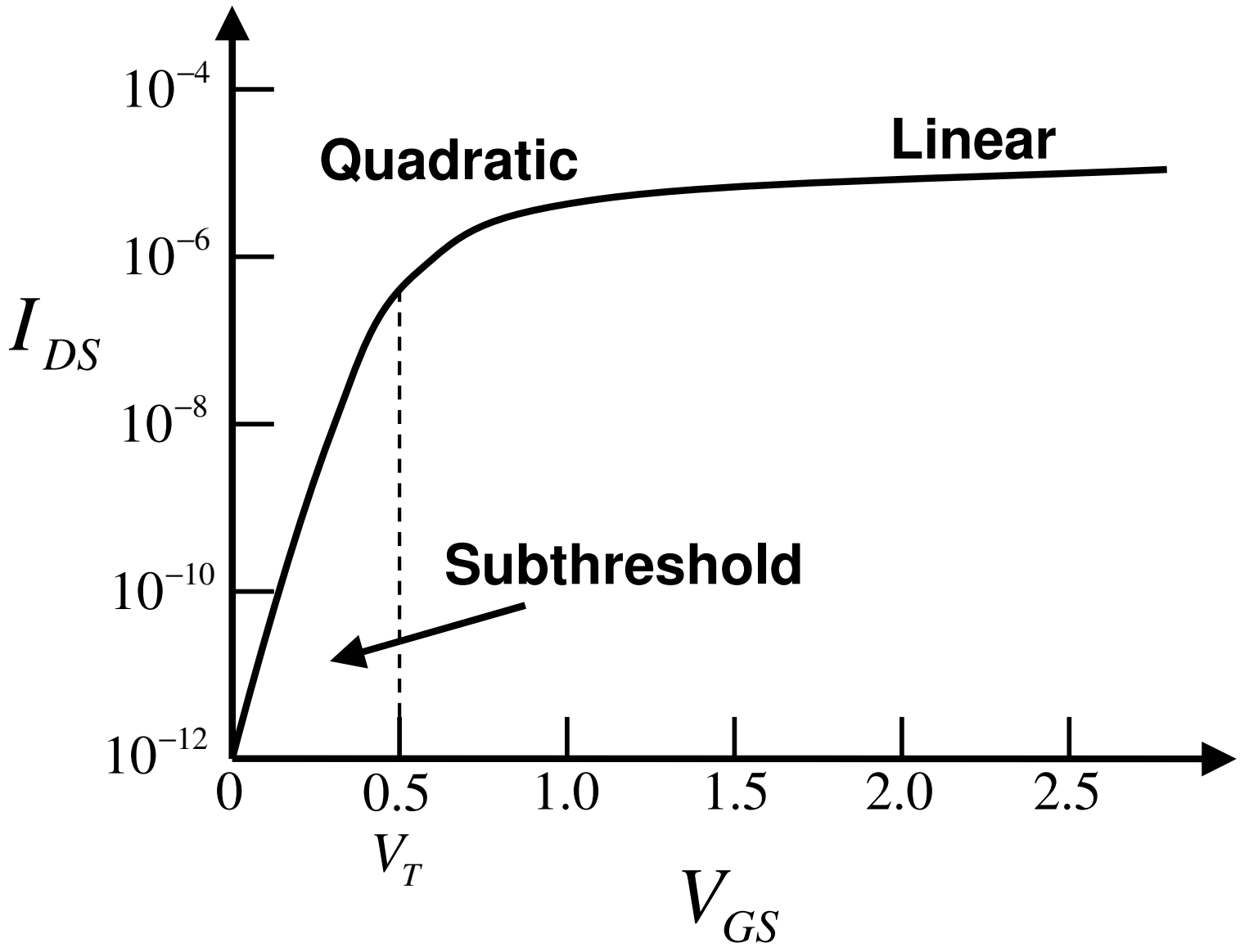
Leakage Currents in Deep Submicron



pn Reverse Bias Current (I1)

- **Reverse-biased pn junction current has two main components**
  - Minority carrier drift near edge of depletion region
  - Electron-hole pair generation in depletion region of reverse-biased junction
  - If both n and p regions doped heavily, Zener tunneling may also be present
- **In MOSFET, additional leakage can occur**
  - Gated diode device action (gate overlap of drain-well pn junctions)
  - Carrier generation in drain-well depletion regions influenced by gate
- **Function of junction area, doping concentration**
- **Minimal contributor to total off current**

Drain Current vs. Gate-Source Voltage



Subthreshold Current Equation

$$I_D = I_S e^{\frac{V_{GS}}{n\,kT/q}} \left(1 - e^{-\frac{V_{DS}}{kT/q}} \right) \left(1 + \lambda V_{DS} \right)$$

- **I_s and *n* are empirical parameters**
- **Typically, $n \geq 1$ often ranging around $n \approx 1.5$**
- **Usually want small subthreshold leakage for digital designs**
  - Define quality metric: inverse rate of decline of current wrt V_{GS} below V_T
  - Subthreshold slope factor *S*: $S = n \frac{kT}{q} \ln(10)$

Detailed Subthreshold Current Equation

$$I_D = A\exp\left(\frac{q}{nkT}\left(V_{GS} - V_{T0} - \gamma V_S + \eta V_D\right)\right)\left(1 - \exp\left(\frac{-qV_{DS}}{kT}\right)\right)$$

$$A = \mu_0 C_{ox}\frac{W}{L}\left(\frac{kT}{q}\right)^2 e^{1.8}$$

- **V_{T0} = zero bias threshold voltage,**
- **$\mu 0$ = zero bias mobility**
- **Cox = gate oxide capacitance per unit area**
- **γ = linear body effect coefficient (small source voltage)**
- **η = DIBL coefficient**

Subthreshold Slope Factor

- **Ideal case: *n* = 1**
  - *S* evaluates to 60 mV/decade (each 60 mV V_{GS} drops below V_T, current drops by 10X)
  - Typically *n* = 1.5 implies slower current decrease at 90 mV/decade
  - Current rolloff further decreased at high temperature, where fast CMOS logic tends to operate
- ***n* determined by intrinsic device topology and structure**
  - Changing n requires different process, like SOI

Subthreshold Slope of Various Processes

Technology	Doping	S (mV / decade)
0.8 μm, 5 V CMOS	LDD	86
0.6 μm, 5 V CMOS	LDD	80
0.35 μm, 3.3 V BiCMOS	LDD	80
0.35 μm, 2.5 V CMOS	HDD	78
0.25 μm, 1.8 V CMOS	HDD	85

- **Roy & Prasad, p. 216**

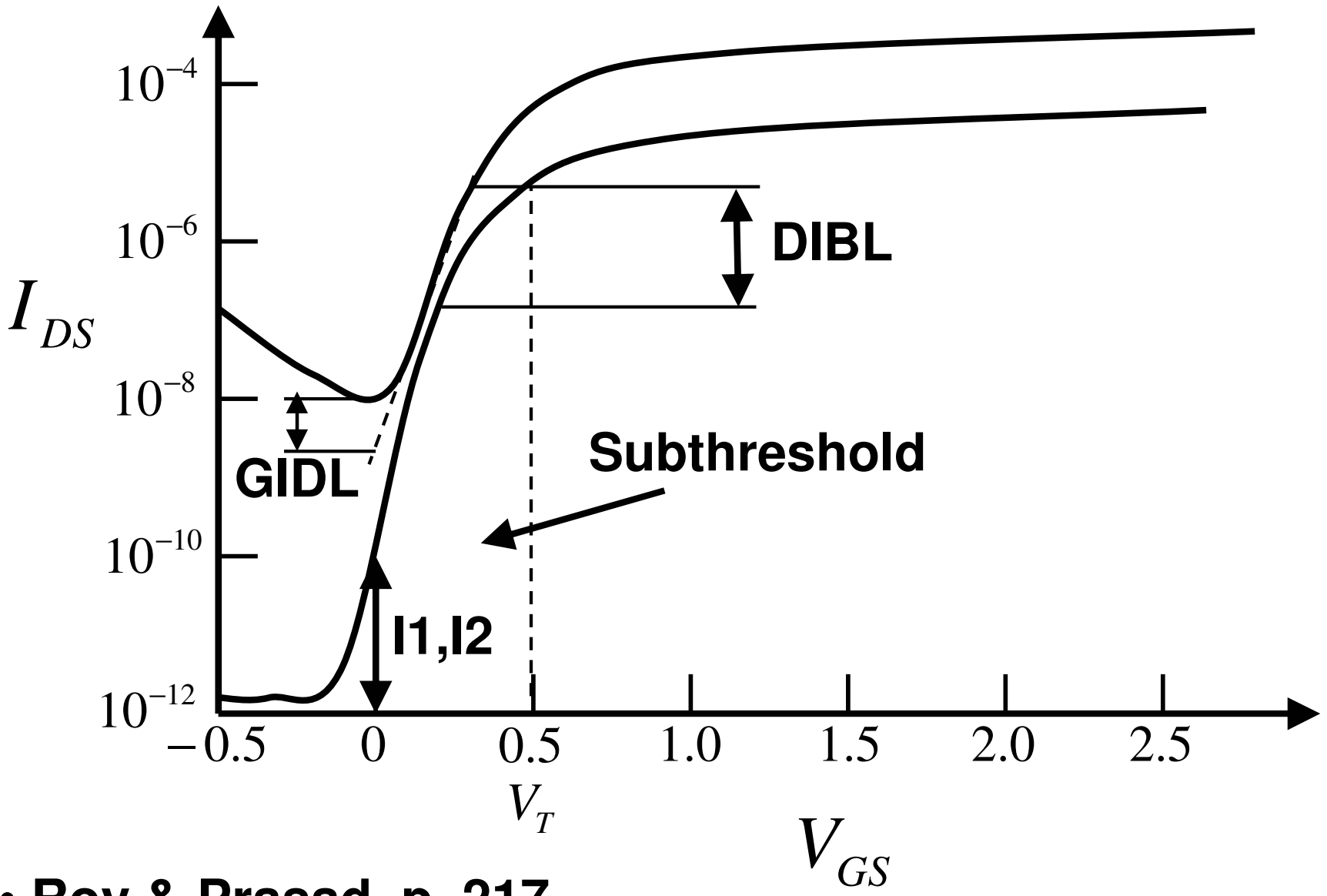
Drain Induced Barrier Lowering (I3)

- **DIBL occurs when drain depletion region interacts with source near channel surface**
  - Lowering source potential barrier
  - Source injects carriers into channel without influence of gate voltage
  - DIBL enhanced at higher drain voltage, shorter effective channel length
  - Surface DIBL happens before deep bulk punchthrough
- **DIBL does not change *S* but lowers V_T**
  - Higher surface, channel doping and shallow junctions reduce DIBL leakage current mechanism

Gate Induced Drain Leakage (I4)

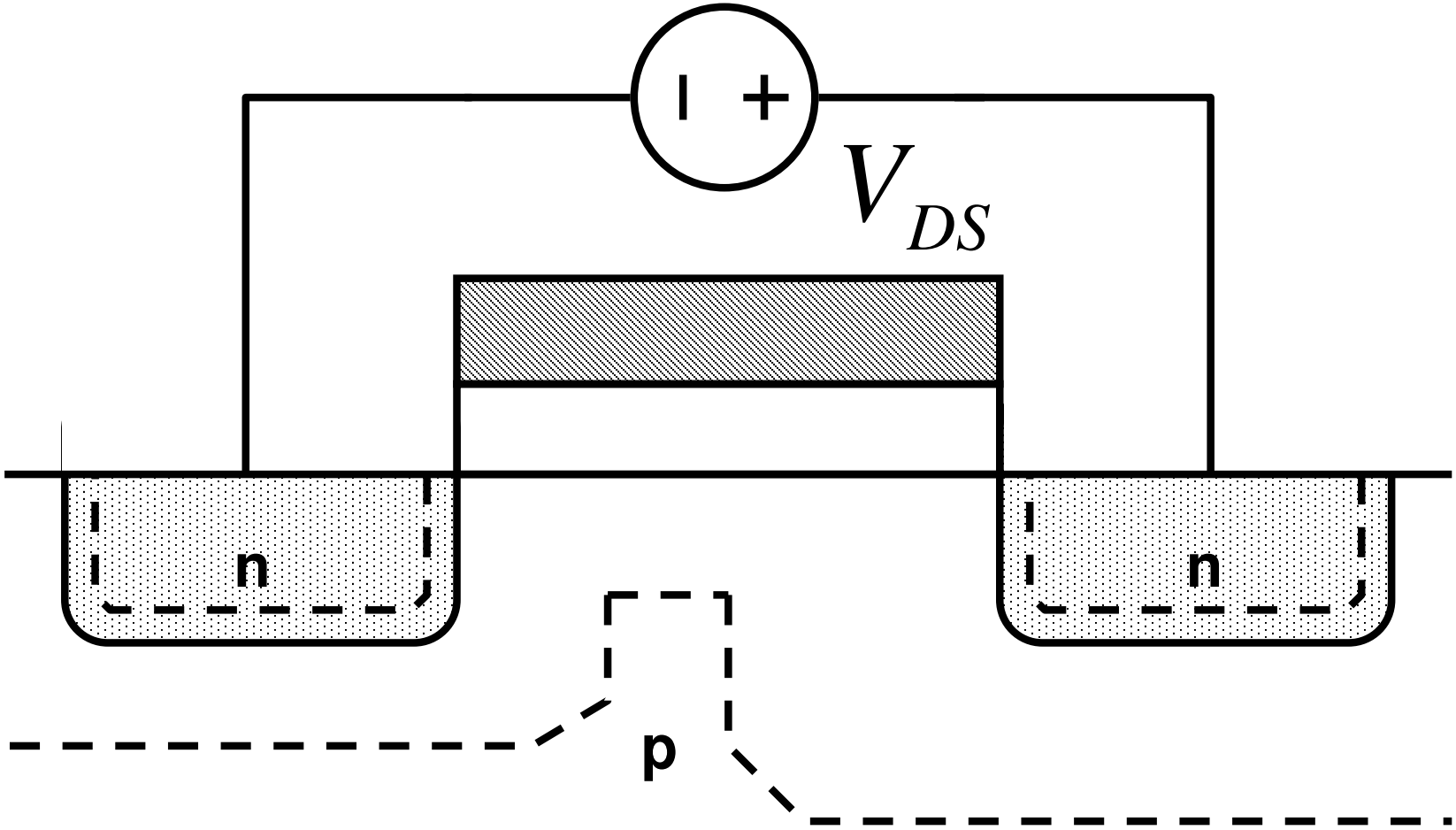
- **GIDL current appears in high E-field region under gate / drain overlap causing deep depletion**
  - Occurs at low V_G and high V_D bias
  - Generates carriers into substrate from surface traps, band-to-band tunneling
  - Localized along channel width between gate and drain
  - Seen as “hook” in I-V characteristic causing increasing current for negative V_G
  - Thinner oxide, higher VDD, lightly-doped drain enhance GIDL
- **Can be major obstacle to reducing off current**

Revised Drain Current vs. Gate Voltage



- **Roy & Prasad, p. 217**

Punchthrough



- **Source / Drain depletion regions "touch" deep inside channel**

Punchthrough Channel Current (I5)

- **Space-charge condition allows channel current to flow deep in subgate region**
  - Gate loses control of subgate channel region
- **Current varies quadratically with drain voltage**
  - Subthreshold slope factor *S* increases to reflect increase in drain leakage
- **Regarded as subsurface version of DIBL**

Gate Oxide Tunneling (I7)

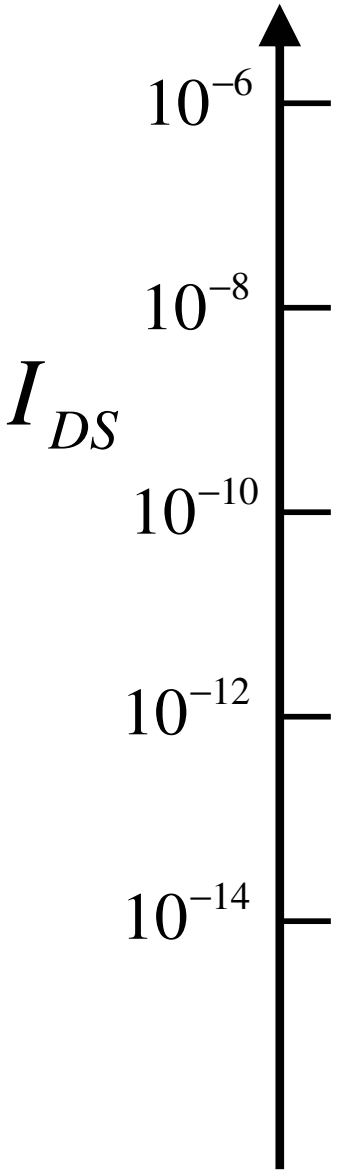
$$I_{OX} = AE_{OX}^{2} e^{-B/E_{OX}}$$

- **High E-field E_{OX} can cause direct tunneling through gate oxide or Fowler-Nordheim (FN) tunneling through oxide bands**
- **Typically, FN tunneling at higher field strength than operating conditions (likely remain in future)**
- **Significant at oxide thickness < 50 Angstroms**
- **Could become dominant leakage mechanism as oxides get thinner**
  - High K dielectrics might make better
  - Interesting circuit design issues (see ISSCC 2004)

Other Leakage Effects

- **Narrow Width Effect (I6)**
  - V_T increases for geometric gate widths around 0.5 μm in non-trench isolated technologies
  - Opposite effect in trench isolated technologies: V_T decreases for widths below 0.5 μm
- **Hot Carrier Injection (I8)**
  - Short channel devices susceptible to energetic carrier injection into gate oxide
  - Measurable as gate and substrate currents
  - Charges are a reliability risk leading to device failure
  - Increased amplitude as length reduced unless V_{DD} scaled accordingly

Leakage Summary



Weak inversion + pn junction + DIBL + GIDL (V_D = 3.9 V)

Weak inversion + pn junction + DIBL (V_D = 2.7 V)

Weak inversion + pn junction (*S* = 80 mV/decade, V_D = 0.1 V)

pn junction

- **Roy & Prasad, p. 219**
- **No punchthrough**
- **No width effect**
- **No gate leakage**

Leakage Current Estimation

$$P_{leak} = \sum_i I_{DS_i} V_{DS_i}$$

- **Parallel transistors, simply add leakage contributions for each one**
- **For series connected devices, calculating leakage currents more complex**
  - Equate subthreshold currents through each device in series stack
  - Solve for V_{DS1} (first device in series stack) in terms of V_{DD} assuming source voltage small
  - Remaining voltages must sum to total voltage drop across series stack